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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/334,238	06/16/1999	MICHAEL L. LONGWELL	JMS009-00	5116

7590 08/01/2005

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EXAMINER	
TU, CHRISTINE TRINH LE	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 08/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/334,238	LONGWELL ET AL.	
	Examiner	Art Unit	
	Christine T. Tu	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed 7/19/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15, 17-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9, 14-15 and 17-35* is/are rejected.

7)☒ Claim(s) *10-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The finality of the action (mailed on April 5, 2005) is withdrawn due to the updated search.

2. Claim 27 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. In other words, limitations of the parity generation circuit in claim 27 are similar to the limitations of parity generation circuit being recited in the independent claim (claim 24).

3. Applicant is advised that should claims 25 and 26 be found allowable, claims 28 and 29 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application

by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 24-25, 27-28 and 31-35 are rejected under 35 U.S.C. 102(e) as being anticipate by McGinn (6,216,251).

Claim 24, 27:

McGinn teaches (figures 1-2) a microcontroller (100) comprising a memory (104). The memory (104) contains an N column by M row memory array (200) coupled to a parity controller (208) and a latch/parity logic (210) via a block of sense amplifiers (204). The memory (104) can perform error checking and correction functions (column 2 lines 15-38 & lines 60-67).

McGinn also teaches the parity controller (208) for comparing the new row parity vector with a previously generated row parity vector. This comparison indicates each row in which an error occurred (column 4 lines 1-9).

McGinn further teaches the parity controller (208) for generating a parity bit for the data stored in each column of the memory array (200) and storing these bits as a column parity vector into the memory array (200) (column 3 lines 46-49).

Claim 25:

McGinn's parity controller (28) compares the new column parity vector with a previously generated column parity vector. This comparison indicates each column in which an error occurred (column 4 lines 12-18).

Claim 28:

Claim 28 is rejected for reasons similar to those set forth against claim 25.

Claim 31:

McGinn teaches (figures 1-2) a microcontroller (100) comprising a memory (104). The memory (104) contains an N column by M row memory array (200) coupled to a parity controller (208) and a latch/parity logic (210) via a block of sense amplifiers (204). The memory (104) can perform error checking and correction functions (column 2 lines 15-38 & lines 60-67).

McGinn also teaches that the parity controller (208) generates a parity bit for the data stored in each row of the memory array (200). The parity controller (208) later compares the new row parity vector with a previously generated row parity vector. This comparison indicates each row in which an error occurred. Then, the combination of the parity controller (208) and the latch/parity logic (210) corrects the error of the failing row (figure 5, column 3 lines 49-52; column 4 lines 1-9; column 7 line9-column 8 line 26).

Claim 32:

McGinn teaches that the combination of parity controller (208) and latch/parity logic (210) detects and sets multiple error flag if more than one error is detected (column 8 lines 45-52).

Claims 33-35:

Claims 33-34 and 35 are rejected for reasons similar to those set forth against claims 31 and 32, respectively.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 26, 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over McGinn (6,216,251).

Claim 26:

McGinn does not explicitly teach the feature of correct the detect column bit error. McGinn, however, teaches that that the combination of parity controller (208) and the latch/parity logic (210) corrects the error in a failing row (figure 5, column 7 line 8-column 8 line 25).

It would have been obvious to one of ordinary skill in the art that McGinn's combination of parity controller (208) and latch/parity logic (210) also encompasses the feature of correcting the error in a failing column. One having ordinary skill in the art would be motivated to do so because McGinn teaches not only the error detection of a failing row, but also the error detection in a failing column (column 4 lines 1-18).

Claim 29:

Claim 29 is rejected for reasons similar to those set forth against claim 26.

Claim 30:

McGinn's microcontroller (100) would have been an IC which comprising the feature of memory error checking and correction (column 2 lines 15-38 & column 1 lines 22-60).

9. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson et al. (6,598,197 and Peterson hereinafter).

Claims 1 & 2:

Peterson teaches the invention substantially as claimed. Peterson discloses (figure 4) a method and apparatus for reading data from a memory device (20). A first set of bits (22a) is read from the memory (20) and a second set of bits (22b) is read from the memory (20) and the two parity bits from the LSB and LSB-1of the memory (20) are all coupled to respective input terminals of an error detector (60') and the error corrector (40). The error detector (60') contains two parity detectors: a first one processing the first set of bits (22a) and the LSB containing the corresponding parity bit P_a; and a second parity detector processing the second set of bits 22b and the LSB-1 containing the corresponding parity bit P_b. If a parity error is detected by either of these parity detectors, a signal is supplied to the error corrector (40) conditioning it to perform error correction (column 4 lines 23-39).

Peterson does not explicitly teach the access circuit. Peterson, however, teaches the buses for carrying the first and the second set of data (22a & 22b) and parity bits (LSB-1 & LSB) to both the error corrector (40) and the error detector (40') (figure 4). It would have been obvious to one skilled in the art at the time the invention was made to name Peterson's buses as an "access circuit". One having ordinary skill in the art would be motivated to do so because naming Peterson's buses as the "access circuit" would not affect the performance of Peterson's buses.

Claim 3:

Peterson's first and second set of bits (22a & 22b) each set is having a 7-bit set (column 4 lines 45-46).

Claim 4:

Peterson's not only teaches the 7-bit detector(s) (60') (figure 4), Peterson also teaches the 5-bit detectors (60'') (figure 6).

Claim 5:

Peterson's memory device (20) would have been a read/write (RAM) memory device (column 1 lines 31-34).

Claims 6 and 7:

These claims are similar to claims 1 and 2 except that the memory comprising memory cells and each cell storing a bit. Well, Peterson teaches that memory device (20) would have been a read/write (RAM) memory device (column 1 lines 31-34). In addition, a RAM comprising memory cells and each cell storing a bit is well-known in the art.

Claims 8 and 9:

Claims 8 and 9 are rejected for reasons similar to those set forth against claims 3 and 7.

10. Claims 14-15 and 17-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carson et al. (5,432,729 and Carson hereinafter) in view of McGinn (6,216,251).

Claim 14, 15, 17-18, 19, 21, 23:

Carson teaches the invention substantially as claimed. Carson teaches an electronic module comprising a multiplicity of stacked IC chips, such as memory chips of (128kx8) SRAM ICs, with active substrate/circuitry. This circuitry includes error detection or correction logic. Carson further teaches that the active substrate provides memory address via its address bus (ADDR0 ... 16) to a 41- layer stack of SRAM ICs (figures 2 & 6, column 3 lines 23-24 & lines 40-65; column 4 lines 54-66; column 9 line 35-column 10 line 45).

Carson does not explicitly teach the row error detection circuit for detecting an error in a bit of a row of the accessed bits and a column error detection circuit for detecting an error in a bit of a column of the accessed bits. McGinn, however, teaches (figures 1-2) a memory comprising a parity controller (28) and a memory array (200) such that the parity controller (208) detects an error in a single row and detects an error in a single column (column 4 lines 1-31).

It would have been obvious to one skilled in the art at the time the invention was made to realize each of Carson's (128kx8) SRAM IC chip would have comprised of McGinn's memory having a parity controller and a memory array. One having ordinary skill in the art would be motivated to do so because Carson's IC chip having detection and correction logic (column 4 lines 54-67).

Claims 20 and 22:

Carson also teaches that the latch parity logic also uses the existing architecture of the memory to perform its memory check and to correct its errors (column 2 lines 26-28).

11. Claims 10-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (571)272-3831. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571)272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christine T. Tu
Primary Examiner
Art Unit 2133

July 26, 2005